

# MOS ANTIFUSE WITH LOW POST-PROGRAM RESISTANCE

## Abstract of the Disclosure

A semiconductor device having an increased intersection perimeter between edge regions of a first conductor and portions of a second conductor is disclosed. In one embodiment, the intersection perimeter is the region where the perimeter of a gate structure overlaps an active area. The intersection perimeter between the conductors directs the breakdown of the dielectric material, increasing the likelihood that the programming event will be successful. In at least one embodiment, the portion of a current path that travels through a highly doped area is increased while the portion that travels through a non-highly doped area is decreased. This decreases post-program resistance, leading to better response time for the device.